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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,267	10/31/2003	Seiichi Watarai	088408/01DIV	9222

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,267	WATARAI, SEIICHI	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,10-12,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,10-12,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/101,936.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 12/17/04.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 3, 10-12, 18 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 2, the phrase "transferring the input data from the data input means to the data latching means" on line 10 is indefinite because the recitation "transferring the input data" in the above phrase is misdescriptive because the input data means (33-34, Figure 2) receiving the input data (D, DB) and providing outputs at the drains of transistors 33 and 34. Thus, the clock synchronization means (31-32) transferring the outputs of the data input means (33-34, i.e., the data at the drains of transistors 33 and 34) to data latch means, i.e., the clock synchronization does not transferring the data input (D, DB). It is suggested that "transferring the input data from the data input means" on line 10 be changed to --transferring outputs of the data input means--.

Also in claim 2, the recitation "a first logic level state" on line 15 is unclear antecedent basis since it is not clear whether the above recitation is the same as "a first logic level" recited earlier in the claim. It appears that "a first logic level state" on line 15 needs to be changed to --a state of said first logic level--. Clarification and/or appropriate correction is required.

With respect to claim 3, the recitations "a second logic level state" and "a first logic level state" on line 14 are unclear antecedent basis since it is not clear whether the above recitations are the same as "a second logic level" and "a first logic level", respectively, recited earlier in the claim. It appears that "a second logic level state" and "a first logic level state" on line 14 need to be changed to --a state of said second logic level-- and --a state of said first logic level--, respectively. Clarification and/or appropriate correction is requested.

Claims 10-12 are indefinite because they include the indefiniteness of claim 2.

Also in claim 10, "via said clock synchronization means" on line 4 is misdescriptive since it is inconsistent with what is disclosed and shown in the drawings, and with what already recited in the independent claim. Note that because the independent claim 2 already recited that the clock synchronization means is for transferring data from the data input means to the data latch means, so the clock synchronization means must be connected in between the data input means and the data latch means, so the embodiment for independent claim 2 is read on Figure 2. Further, Figure 2 clearly shows the sources of the transistors (33, 34) of the data input means (33, 34) directly coupled to a power source (ground GND), so the recitation that the sources of both first and second NMOS transistors of the data input means being coupled to a power source "via said clock synchronization means" is misdescriptive. It is suggested that "via said clock synchronization means" be deleted.

Also in claim 10, it is suggested that "constituting the input data appears" on both lines 10 and 14 be changed to --constituting the outputs of the data input means appears-- for the reason as discussed in claim 2 above (see discussion with regard to the "transferring the input data").

Also in claim 11, "via said input data means" recited on both lines 4 and 6 is indefinite finite because it is inconsistent with what is disclosed as shown.. Note that as discussed above, the embodiment for independent claim 2 is read on Figure 2 (see discussion in claim 10), and it is clearly seen in Figure 2 that clock synchronization means (31, 32) comprising first and second NMOS transistors (31, 32) each having a source directly connected to the respective drain terminal of transistors (33, 34) of the data input means, i.e., not "via said input data means". Thus, it is suggested that ", via said data input means," on both lines 4 and 6-7 be deleted.

Also in claim 11, "constituting the input data appears" on both lines 5 and 8 must be changed to --constituting the outputs of the data input means appears-- for the similar reason as discussed in claim 10 above.

Also in claim 11, "a common terminal" on lines 4, 7, 9 and 10 are indefinite because they are unclear antecedent basis since it is not clear whether they are the same common terminal or not. It is suggested that "a common terminal" on lines 4, 7, 9 and 10 must be changed to --a first common terminal--, --a second common terminal--, --a third common terminal--, and --a fourth common terminal--, respectively.

Also in claim 12, the recitation "via said clock synchronization means" on line 4 is misdescriptive since it is inconsistent with what is disclosed and shown. Note that as discussed above, the embodiment for independent claim 2 is read on Figure 2 (see discussion in claim 10), and it is clearly seen in Figure 2 that the latch enhancement means (35, 36) comprising NMOS transistors (35, 36) having their sources directly connected to a power source (ground GND), so it is suggested that "via said clock synchronization means" on line 4 be deleted.

Also in claim 12, the recitations "a common terminal" on lines 7-8 and 10-11 are indefinite because they are unclear antecedent basis since it is not clear whether they are the same common terminal or not. It is suggested that "a common terminal" on lines 7-8 and 10-11 must be changed to --a first common terminal-- and --a second common terminal--,respectively.

Also in claim 11, "constituting the input data appears" on both lines 8 and 12 must be changed to --constituting the outputs of the data input means appears-- for the similar reason as discussed in claim 10 above.

With respect to claim 18, the recitation "transfers the input data from the input unit" on line is indefinite for the similar reason as discussed in claim 2 above. It is suggested that "transfers outputs of the input unit". Also "a first logic level state" on line 13 is indefinite for the similar reason as discussed in claim 2, and it appears that "a first logic level state" on line 13 needs to be changed to --a state of the first logic level--.

With respect to claim 19, the recitations "a second logic level state" and "a first logic level state" on the last line are indefinite for the similar reason as discussed in claim 3 above, and it appears that "a second logic level state" and "a first logic level state" on the last line need to be changed to --a state of said second logic level-- and --a state of said first logic level--, respectively. Clarification and/or appropriate correction is requested.

Allowable Subject Matter

4. Claims 2, 3, 10-12, 18 and 19 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 18, 2005

Long Nguyen
Primary Examiner
Art Unit: 2816